

FIG. 1



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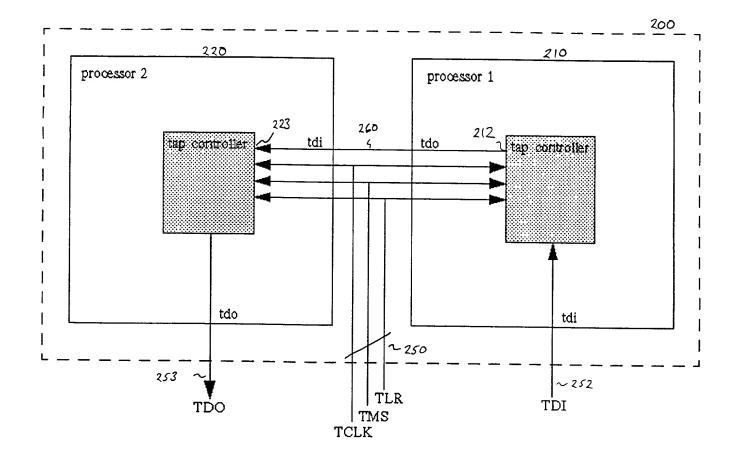
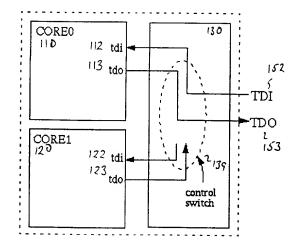
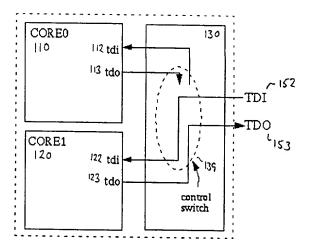
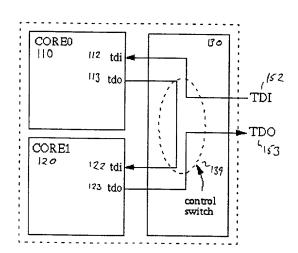


FIG. 2







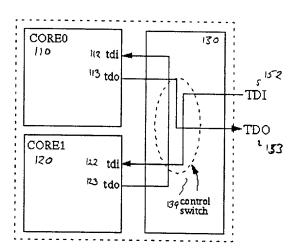
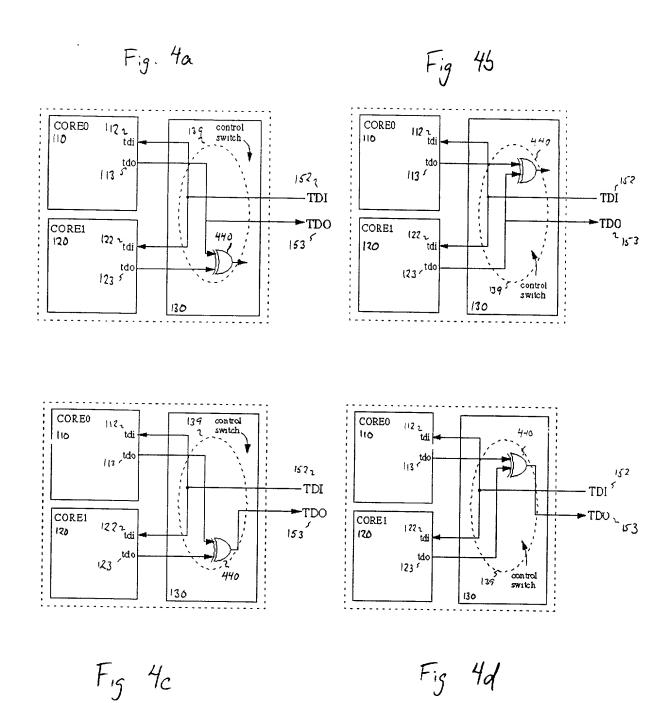


Fig 3c

Fis 3d



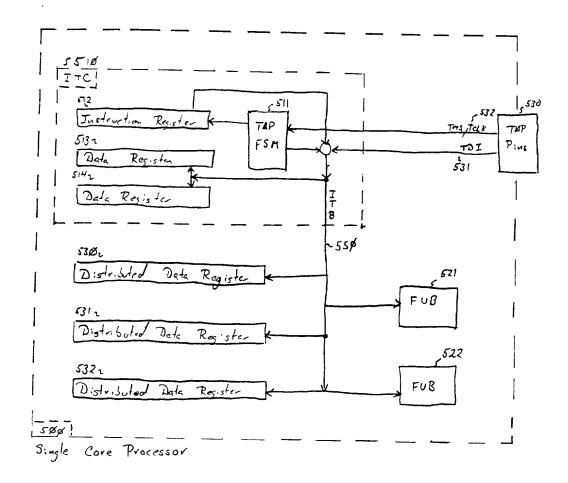
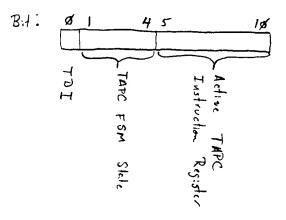


Fig. 5

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## Fig. 6



Integrated Test Bus

Fig. 7

TAP Core Configuration Register

Davallel Configuration

Serial Configuration

Independent Configuration

Controlling TAPC

Bit

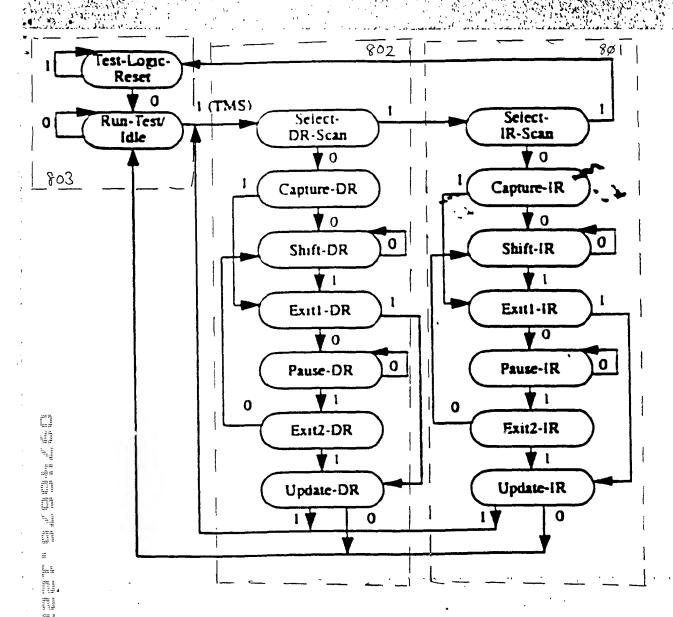


Fig. 8

